Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1. (currently amended) A method for improving high-speed output buffer components comprising the steps of:

establishing a cascode transistor module comprising two transistors, each of which has a control input and first and second current terminals,

establishing a differential pair module comprising two transistors, each of which has a control input and first and second current terminals,

said cascode module connected to receive~~for receiving~~ at its second current terminals a substantially differential current signal from the first terminals of said ~~a~~ differential pair module and to transmit ~~transmitting~~ at its first current terminals said substantially differential current signal into a pair of external load impedances as a first output waveform and a second output waveform; and~~,~~

engineering the resistive loads seen by the first terminals ~~output nodes~~ of said differential pair module, based on one or more criteria thereby engineering the symmetry between the rising edge and the falling edge for each of said first output waveform and said second output waveform.

2. (currently amended) The method of claim 1 wherein said cascode transistor module's two transistors comprise~~s~~ first and second bipolar transistors, said cascode transistor module's first current terminals being the collectors of said first and

second bipolar transistors and said cascode transistor module's second current terminals being the emitters of said first and second bipolar transistors.

3. (currently amended) The method of claim 1 wherein said cascode transistor module's two transistors comprise~~s~~ first and second field effect transistors (FETs), said cascode transistor module's first current terminals being the drains of said first and second FETs and said cascode transistor module's second current terminals being the sources of said first and second FETs.

4. (currently amended) The method of claim 1 wherein said differential pair module's two transistors comprise~~s~~ first and second bipolar transistors, said differential pair module's first current terminals being the collectors of said first and second bipolar transistors and said differential pair transistor module's second current terminals being the emitters of said first and second bipolar transistors.

5. (cancelled) The method of claim 4 wherein said output nodes of said differential pair module comprise the collector nodes of said bipolar transistors and the input nodes of said differential pair module comprise the base nodes of said bipolar transistors.

6. (currently amended) The method of claim 1 wherein said differential pair module's two transistors comprise~~s~~ first and second field effect transistors (FETs), said differential pair module's first current terminals being the drains of said first and second FETs and said differential pair module's second current terminals being the sources of said first and second

FETs.

7. (cancelled) The method of claim 6 wherein said output nodes of said differential pair module comprise the drain nodes of said field effect transistors (FETs) and the input nodes of said differential pair module comprise the gate nodes of said field effect transistors.

8. (currently amended) The method of claim 1 wherein the step of engineering the resistive loads comprises the step of ~~inserting~~ connecting a first resistive module between said cascode transistor module and said differential pair module such that said resistive module conducts said substantially differential current signal.

9. (currently amended) The method of claim 8 wherein said first resistive module comprises a first resistor connected between the first terminal of one of said differential pair module transistors and the second terminal of one of said cascode module transistors, and a second resistor connected between the first terminal of the other of said differential pair module transistors and the second terminal of the other of said cascode module transistors~~in a parallel configuration~~.

10. (original) The method of claim 9 wherein said first resistor and said second resistor have substantially identical characteristics.

11. (original) The method of claim 1 wherein the step of engineering the resistive loads comprises the step of selecting a cascode bias voltage for said cascode transistor module.

12. (currently amended) The method of claim 11 wherein the wherein the step of engineering the resistive loads comprises selecting resistance values for said loads to obtain a desired range $V_{io,max} - V_{io,min}$, where V_{io} is the voltage between the control input and the first terminal of a differential pair module transistor~~suppressing the voltages at the outputs of said differential pair module by increasing the maximum range of values for said differential pair module's input voltages and output voltages~~.

13. (currently amended) The method of claim 11 wherein the step of engineering the resistive loads comprises selecting a cascode bias voltage to obtain a desired rate of change of C_{io} as a function of V_{io}, where C_{io} is the capacitance between the control input and the first terminal of a differential pair module transistor and V_{io} is the voltage between the control input and the first terminal of a differential pair module transistor~~suppressing the voltages at the outputs of said differential pair module by increasing the degree of non-linearity of the input-output capacitance of the differential pair module transistors as a function of the input-output voltage of said differential pair module transistors~~.

14. (currently amended) A method for improving high-speed output buffer components comprising the steps of: ~~The method of claim 1 further comprising the step of~~

establishing a cascode transistor module comprising two transistors, each of which has a control input and first and second current terminals;

establishing a differential pair module comprising two transistors, each of which has a control input and first and second current terminals;

said cascode module connected to receive at its second current terminals a substantially differential current signal from the first terminals of said differential pair module and to transmit at its first current terminals said substantially differential current signal into a pair of external load impedances as a first output waveform and a second output waveform;

engineering the resistive loads seen by the first terminals of said differential pair module, based on one or more criteria thereby engineering the symmetry between the rising edge and the falling edge for each of said first output waveform and said second output waveform; and

preconditioning the signal input applied to said differential pair module's control inputs.

15. (currently amended) The method of claim 14 wherein the step of preconditioning the ~~signal comprises the step of preconditioning the~~ signal input to said differential pair module comprises using one or more stages selected from the list of:

an amplifier;

a limiting amplifier;

a buffer; and

a Cherry-Hooper amplifier.

16. (currently amended) A method for improving high-speed output buffer components comprising the steps of: ~~The method of claim 1 further comprising the steps of~~

establishing a cascode transistor module comprising two transistors, each of which has a control input and first and second current terminals;

establishing a differential pair module comprising two transistors, each of which has a control input and first and second current terminals

second current terminals;

said cascode module connected to receive at its second current terminals a substantially differential current signal from the first terminals of said differential pair module and to transmit at its first current terminals said substantially differential current signal into a pair of external load impedances as a first output waveform and a second output waveform;

engineering the resistive loads seen by the first terminals of said differential pair module, based on one or more criteria thereby engineering the symmetry between the rising edge and the falling edge for each of said first output waveform and said second output waveform; and

establishing a driving stage which provides a signal input to the control inputs of the transistors of said differential pair module, and engineering the output resistance of said ~~due to the~~ driving stage~~driving the input to said differential pair module~~.

17. (currently amended) The method of claim 16 wherein the step of engineering the output resistance of said driving ~~due to the~~ stage ~~driving the input to said differential pair module~~ comprises engineering the symmetry between the rising edge and the falling edge for each of ~~said differential pair module's input~~ the signal input voltages supplied to the control inputs ~~nodes~~ of the transistors of said differential pair module.

18. (currently amended) The method of claim 16 wherein the step of engineering the output resistance of said driving ~~due to the~~ stage ~~driving the input to said differential pair module~~ comprises one or more steps selected from the list of steps consisting of:

~~coupling~~ connecting a second resistive module in series between said driving stage and ~~to~~ the control input ~~node~~ of one of the ~~first~~ transistors of ~~in~~ said differential pair; and,

~~coupling~~ connecting a third resistive module in series between said driving stage and ~~at~~ the control input ~~node~~ of the other~~second~~ transistor of~~in~~ said differential pair.

19. (currently amended) The method of claim 18 wherein said second resistive module and said third resistive module are substantially identical.

20. (currently amended) The method of claim 18 wherein said second resistive module and said third resistive module comprise one or more resistors.

21. (currently amended) A method for improving high-speed output buffer components comprising the steps of: ~~The method of claim 1~~

establishing a cascode transistor module comprising two transistors, each of which has a control input and first and second current terminals;

establishing a differential pair module comprising two transistors, each of which has a control input and first and second current terminals;

said cascode module connected to receive at its second current terminals a substantially differential current signal from the first terminals of said differential pair module and to transmit at its first current terminals said substantially differential current signal into a pair of external load impedances as a first output waveform and a second output waveform; and

engineering the resistive loads seen by the first terminals

of said differential pair module, based on one or more criteria thereby engineering the symmetry between the rising edge and the falling edge for each of said first output waveform and said second output waveform;

wherein said pair of external load impedances comprise one or more inductive modules.

22. (currently amended) The method of claim 1 wherein the symmetry between the rising edge and the falling edge for each of said first output waveform and said second output waveform is optimized to achieve a symmetrical output waveform.

23. (currently amended) The method of claim 1 wherein the symmetry between the rising edge and the falling edge for each of said first output waveform and said second output waveform is optimized to achieve an asymmetrical output waveform.

24. (currently amended) An improved high-speed output buffer component comprising:

a cascode transistor module comprising two transistors, each of which has a control input and first and second current terminals;

a differential pair module comprising two transistors, each of which has a control input and first and second current terminals, said cascode transistor module arranged to receive at its second current terminals ~~for receiving~~a substantially differential current signal from ~~a~~the first terminals of said differential pair module and to transmit ~~transmitting~~ at its first current terminals said substantially differential current signal into a pair of external load impedances as a first output waveform and a second output waveform, wherein said cascode transistor module further comprises:

a resistive load comprising first and second resistances, said first resistance connected between the first terminal of one of said differential pair module transistors and the second terminal of one of said cascode module transistors, and said second resistance connected between the first terminal of the other of said differential pair module transistors and the second terminal of the other of said cascode module transistors ~~at the input nodes of said cascode transistor module~~; and

a cascode bias voltage node for applying a cascode bias voltage to the control inputs of said cascode transistor module transistors, wherein the symmetry between the rising edge and the falling edge for each of said first output waveform and said second output waveform may be altered by careful selection of one or more elements selected from the list of:

said resistive load, and

said cascode bias voltage.

25. (currently amended) The improved high-speed output buffer component of claim 24 wherein said first and second resistances~~resistive load at the input nodes of said cascode transistor module~~ are due to the intrinsic properties of the differential pair module and the cascode transistor module transistors~~elements~~.

26. (currently amended) The improved high-speed output buffer component of claim 24 wherein said first and second resistances comprise first and second resistors, respectively~~further comprising a first resistive module coupled between said cascode transistor module and said differential pair module for increasing the resistive load at input nodes of said cascode transistor module~~.

27. (cancelled) The improved high-speed output buffer component of claim 26 wherein said first resistive module comprises a first resistor and a second resistor in a parallel configuration.

28. (currently amended) The improved high-speed output buffer component of claim 26~~27~~ wherein said first resistor and said second resistor have substantially identical characteristics.

29. (currently amended) The improved high-speed output buffer component of claim 24 wherein said cascode bias voltage is engineered to obtain a desired range $V_{io,max} - V_{io,min}$, where V_{io} is the voltage between the control input and the first terminal of a differential pair module transistor~~to suppress the voltages at the outputs of said differential pair module~~.

30. (currently amended) The improved high-speed output buffer component of claim 24 wherein said cascode transistor module's two transistors comprise~~s~~ first and second bipolar transistors, said cascode transistor module's first current terminals being the collectors of said first and second bipolar transistors and said cascode transistor module's second current terminals being the emitters of said first and second bipolar transistors.

31. (currently amended) The improved high-speed output buffer component of claim 24 wherein said cascode transistor module's two transistors comprise~~s~~ first and second field effect transistors (FETs), said cascode transistor module's first current terminals being the drains of said first and second FETs and said cascode transistor module's second current terminals

being the sources of said first and second FETs.

32. (currently amended) The improved high-speed output buffer component of claim 24 wherein said differential pair module's two transistors comprise~~s~~ first and second bipolar transistors, said differential pair module's first current terminals being the collectors of said first and second bipolar transistors and said differential pair transistor module's second current terminals being the emitters of said first and second bipolar transistors.

33. (cancelled) The improved high-speed output buffer component of claim 32 wherein said output nodes of said differential pair module comprise the collector nodes of said bipolar transistors and the input nodes of said differential pair comprise the base nodes of said bipolar transistors.

34. (currently amended) The improved high-speed output buffer component of claim 24 wherein said differential pair module's two transistors comprise~~s~~ first and second field effect transistors (FETs), said differential pair module's first current terminals being the drains of said first and second FETs and said differential pair module's second current terminals being the sources of said first and second FETs.

35. (cancelled) The improved high-speed output buffer component of claim 34 wherein said output nodes of said differential pair module comprise the drain nodes of said field effect transistors (FETs) and said input nodes of said differential pair module comprise the gate nodes of said field effect transistors.

36. (currently amended) The improved high-speed output buffer component of claim 24 further comprising ~~one or more circuit elements selected from the list of:~~

~~a keep alive transistor and~~

a bleed resistor connected between the second current terminals of said cascode transistor module's transistors.

37. (currently amended) An improved high-speed output buffer component comprising: ~~The improved high speed output buffer component of claim 24 wherein:~~

a cascode transistor module comprising two transistors, each of which has a control input and first and second current terminals;

a differential pair module comprising two transistors, each of which has a control input and first and second current terminals, said cascode transistor module arranged to receive at its second current terminals a substantially differential current signal from the first terminals of said differential pair module and to transmit at its first current terminals said substantially differential current signal into a pair of external load impedances as a first output waveform and a second output waveform, wherein said cascode transistor module further comprises:

a resistive load comprising first and second resistances, said first resistance connected between the first terminal of one of said differential pair module transistors and the second terminal of one of said cascode module transistors, and said second resistance connected between the first terminal of the other of said differential pair module transistors and the second terminal of the other of said cascode module transistors; and

a cascode bias voltage node for applying a cascode bias voltage to the control inputs of said cascode transistor module transistors, wherein the symmetry between the rising edge and the falling edge for each of said first output waveform and said second output waveform may be altered by careful selection of one or more elements selected from the list of:

said resistive load, and

said cascode bias voltage; and

~~said differential pair module comprises a pair of differential pair module inputs for receiving a differential input signal; and,~~

one or more stages for preconditioning a ~~said~~ differential input signal applied ~~are coupled~~ to said ~~pair of~~ differential pair module's control inputs.

38. (currently amended) The improved high-speed output buffer component of claim 37 wherein said preconditioning stages comprise one or more stages selected from the list of:

an amplifier;

a limiting amplifier;

a buffer; and

a Cherry-Hooper amplifier.

39. (currently amended) The improved high-speed output buffer component of claim 24 further comprising one or more inductive modules coupled to the first terminals ~~outputs~~ of said cascode transistor module.

40. (currently amended) The improved high-speed output buffer component of claim 24 ~~wherein said differential pair module comprises a first transistor with a first input node and a second transistor with a second input node and wherein said~~

~~improved high speed output buffer further comprises one or more elements selected from the list consisting of:~~further comprising:

a driving stage which provides a signal input to the control inputs of the transistors of said differential pair module;

a second resistive module connected in series between said driving stage and ~~coupled to~~ the control input ~~node~~ of one of said ~~first~~ differential pair module transistors; and~~,~~

a third resistive module connected in series between said driving stage and~~coupled to~~ the control input ~~node~~ of the other of said differential pair module ~~second~~ transistors;

said second and third resistive modules ~~thereby engineering~~ engineered to obtain a desired ~~the resistance due to the stage driving the input to said differential pair module and thereby engineering the~~ symmetry between the rising edge and the falling edge for each of said first output waveform and said second output waveform.

41. (currently amended) The improved high-speed output buffer component of claim 40 wherein said second resistive module and said third resistive module are substantially identical.

42. (currently amended) The improved high-speed output buffer component of claim 40 wherein said second resistive module and said third resistive module comprise one or more resistors.

43. (cancelled) A system comprising:

one or more devices coupled to

the improved high-speed output buffer component of claim 24.

44. (cancelled) The system of claim 43 wherein said devices comprise one or more selected from the list of:

broad-band amplifiers;

high-speed logic gates;
narrow-band amplifiers;
amplifiers;
logic gates;
mixers; and
oscillators.

45. (cancelled) The system of claim 43 wherein said system comprises one or more selected from the list of:

wireless local area networks;
networks;
satellite communications devices;
communications systems;
global positioning systems; and
high-speed communication systems.